SHRI VENKATESHWARA UNIVERSITY

Syllabus

M.TECH (VLSI) PART TIME

(Two Years Post Graduation Programme)

III SEMESTER
(w.e.f. 2019-20)

SCHOOL OF ENGINEERING & TECHNOLOGY

SEMESTER-III													
Sl. No.	**Subject Codes**	**Subject**	**Periods**			**Evaluation Scheme**				**End Semester**		Total	Credit
			L	T	P	CT	TA	Total	PS	TE	PE		
1	WVI-301	RTL Simulation and Synthesis with PLDs	3	0	0	20	10	30		70		100	3
2	WVI-031	Parallel Processing	3	0	0	20	10	30		70		100	3
3	WVI-311	RTL Simulation and Synthesis with PLDs Lab	0	0	4				25		25	50	2
4	MLC-301	Research Methodology and IPR	2	0	0	20	10	30		70		100	2
		Total										350	10

Code	Course Name	L-T-P	Cr.
WVI-301	RTL Simulation and Synthesis with PLDs	3-0-0	3

Course Outcomes: At the end of the course, students will demonstrate the ability to:

- Familiarity of Finite State Machines, RTL design using reconfigurable logic.
- Design and develop IP cores and Prototypes with performance guarantees
- Use EDA tools like Cadence, Mentor Graphics and Xilinx.

Syllabus Contents:

Unit1: Top down approach to design, Design of FSMs (Synchronous and asynchronous), Static timing analysis, Meta-stability, Clock issues, Need and design strategies for multi- clock domain designs.

Unit 2: Design entry by Verilog/VHDL/FSM, Verilog AMS.

Unit 3: Programmable Logic Devices, Introduction to ASIC Design Flow, FPGA, SoC, Floor planning, Placement, Clock tree synthesis, Routing, Physical verification, Power analysis, ESD protection.

Unit 4: Design for performance, Low power VLSI design techniques. Design for testability.

Unit 5: IP and Prototyping: IP in various forms: RTL Source code, Encrypted Source code, Soft IP, Netlist, Physical IP, Use of external hard IP during prototyping.

Unit 6: Case studies and Speed issues.

References:

- Richard S. Sandige, “Modern Digital Design”, MGH, International Editions.
- Donald D Givone, “Digital principles and Design”, TMH Charles Roth, Jr. and Lizy K John, “Digital System Design using VHDL”, Cengage Learning.
- Samir Palnitkar, “Verilog HDL, a guide to digital design and synthesis”, Prentice Hall.
- Doug Amos, Austin Lesea, Rene Richter, “FPGA based prototyping methodology manual”, Xilinx

- Bob Zeidman, “Designing with FPGAs & CPLDs”, CMP Books.

Code	Course Name	L-T-P	Cr.
WVI-311	RTL Simulation and Synthesis with PLDs Lab	0-0-4	2

Course Outcomes: At the end of the laboratory work, students will be able to:

- Identify, formulate, solve and implement problems in signal processing, communication systems etc using RTL design tools.
- Use EDA tools like Cadence, Mentor Graphics and Xilinx.

List of Experiments:

1) Verilog implementation of 8:1 Mux/Demux, Full Adder, 8-bit Magnitude comparator, Encoder/decoder, Priority encoder, D-FF, 4-bit Shift registers (SISO, SIPO, PISO, bidirectional), 3-bit Synchronous Counters, Binary to Gray converter, Parity generator.
2) Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.
3) Vending machines - Traffic Light controller, ATM, elevator control.
4) PCI Bus & arbiter and downloading on FPGA.
5) UART/ USART implementation in Verilog.
6) Realization of single port SRAM in Verilog.
7) Verilog implementation of Arithmetic circuits like serial adder/ subtractor, parallel adder/subtractor, serial/parallel multiplier.
8) Discrete Fourier transform/Fast Fourier Transform algorithm in Verilog.

Code	Course Name	L-T-P	Cr.
MLC-301	Research Methodology and IPR	2-0-0	2

Course Outcomes: At the end of this course, students will be able to

- Understand research problem formulation.
- Analyze research related information
- Follow research ethics
- Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

Syllabus Contents:

Unit 1: Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations.

Unit 2: Effective literature studies approaches, analysis Plagiarism, Research ethics,

Unit 3: Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

Unit 4: Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Processof Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

Unit 5: Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

Unit 6: New Developments in IPR: Administration of Patent System. New developmentsin IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

References:

- Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
- Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
- Ranjit Kumar, 2nd Edition , "Research Methodology: A Step by Step Guide for beginners"
- Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
- Mayall , "Industrial Design", McGraw Hill, 1992.
- Niebel , "Product Design", McGraw Hill, 1974.
- Asimov , "Introduction to Design", Prentice Hall, 1962.
- Robert P. Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in New Technological Age", 2016.
- T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

Code	Course Name	L-T-P	Cr.
WVI-031	Parallel Processing	3-0-0	3

Course Outcomes: At the end of this course, students will be able to

- Identify limitations of different architectures of computer
- Analysis quantitatively the performance parameters for different architectures.
- Investigate issues related to compilers and instruction set based on type of architectures.

Syllabus Contents:

Unit 1: Overview of Parallel Processing and Pipelining, Performance analysis,Scalability

Unit 2: Principles and implementation of Pipelining, Classification of pipeliningprocessors, Advanced pipelining techniques, Software pipelining.

Unit 3: VLIW processors
Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC,MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture.

Unit 4: Multithreaded Architecture, Multithreaded processors, Latency hidingtechniques, Principles of multithreading, Issues and solutions

Unit 5: Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, DataParallel Programming, Parallel Software Issues

Unit 6: Operating systems for multiprocessors systems Customizing applications onparallel processing platforms.

References:

- Kai Hwang, Faye A. Briggs, "Computer Architecture and Parallel Processing", MGH International Edition
- Kai Hwang, "Advanced Computer Architecture", TMH
- V. Rajaraman, L. Sivaram Murthy, "Parallel Computers", PHI.
- William Stallings, "Computer Organization and Architecture, Designing for performance" Prentice Hall, Sixth edition
- Kai Hwang, Zhiwei Xu, "Scalable Parallel Computing", MGH
- David Harris and Sarah Harris, "Digital Design and Computer Architecture", Morgan Kaufmann.